8-bit data register

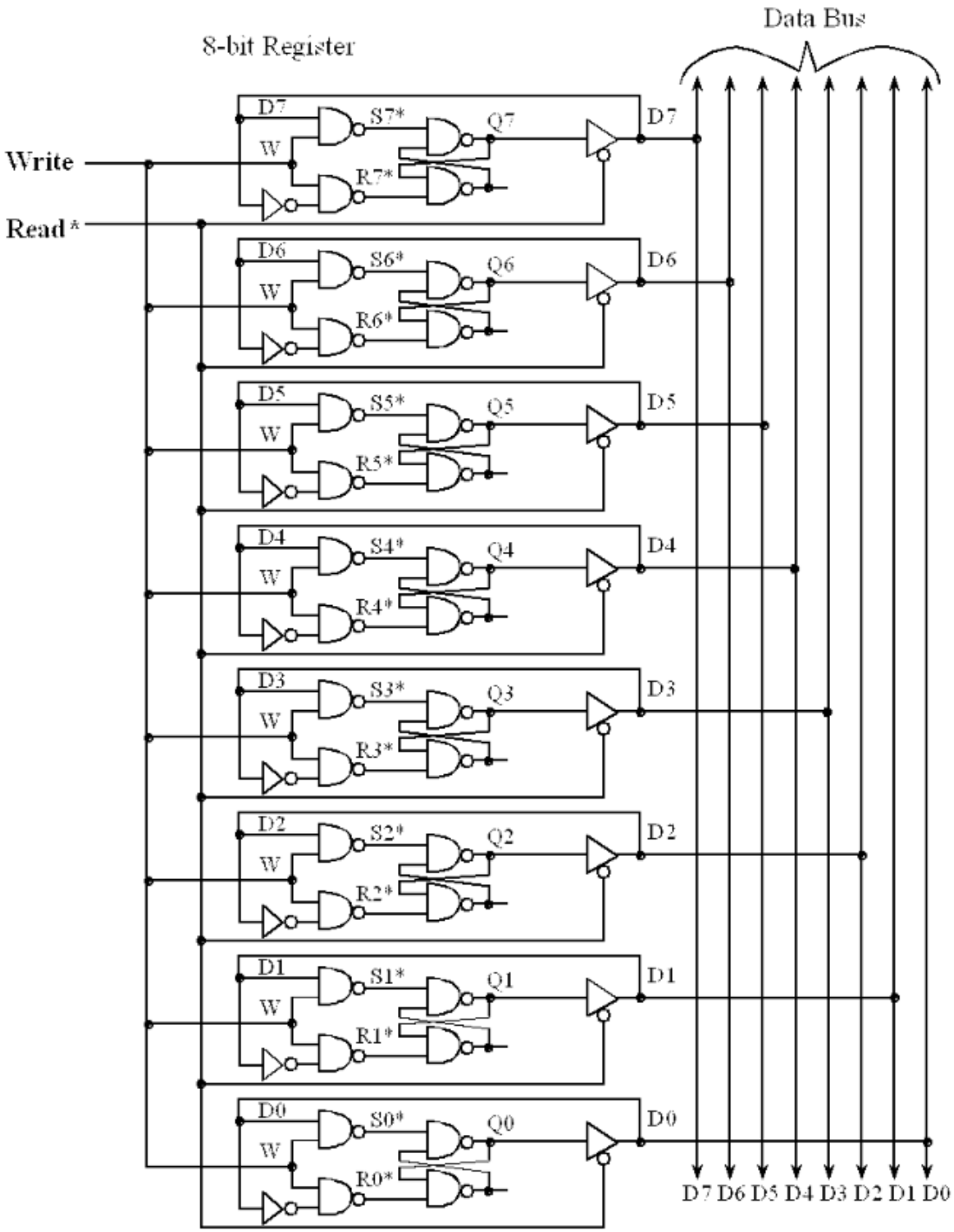

Figure 4.13. Digital logic implementation of a register.

Figure 1. 8 bit data register. Image credit: http://users.ece.utexas.edu/~valvano/Volume1/E-Book/C4_DigitalLogic.htm

4x3 RAM Cell

1. CS = chip select (active high)
2. RD = read mode (active low)
3. OE = output enable (active high);
4. A_0, A_1 = address bits
5. I_0, I_1, I_2 = data input bits (for writes only)
6. O_1, O_2, O_3 = output bits (for reads only)