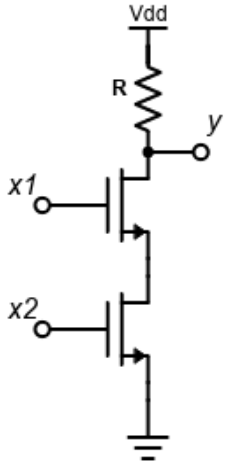
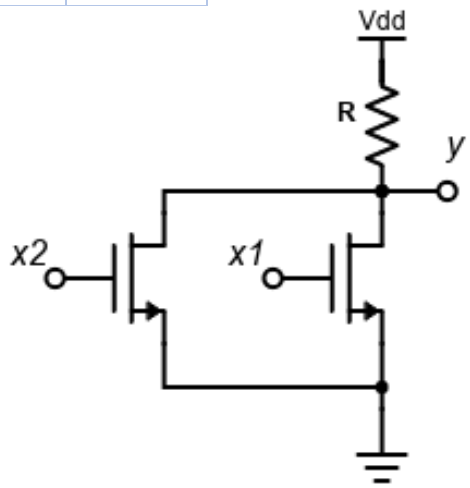
Logic Cate Worksheet (Engn/Phys 208) winter 2021

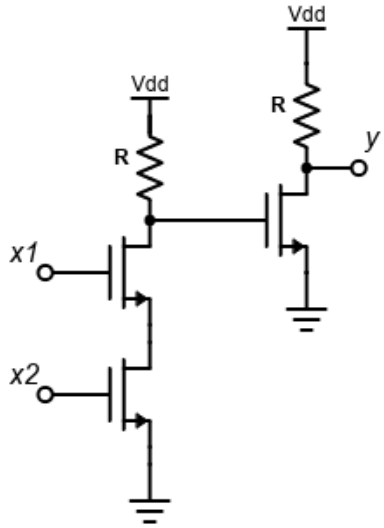
NMOS Logic Gates

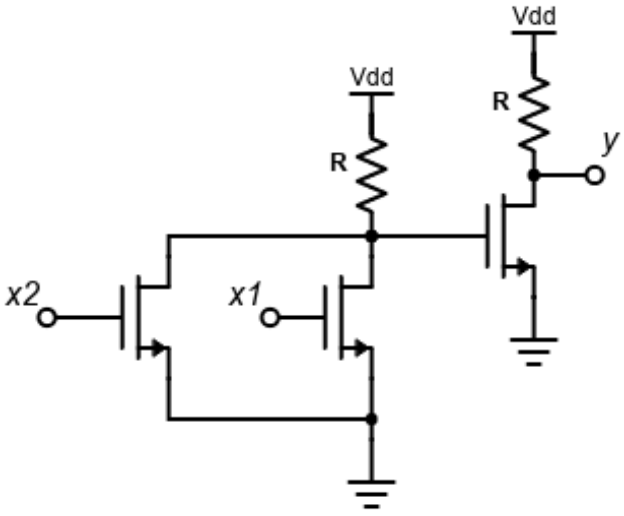
1. For each logic gate below (Circuits A-D), consider the 4 input combinations (*x1, x2*): Determine the state of the MOSFETs (on/off)
2. Determine the output state *y* (0/1) in each case.
3. Complete the truth table (e.g. see below). Propose a name for the gate based on the logic implemented

x1	x2	y



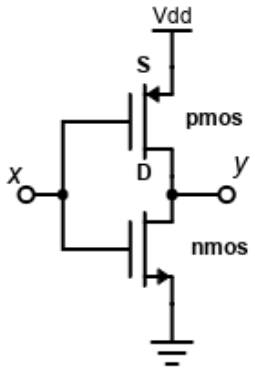






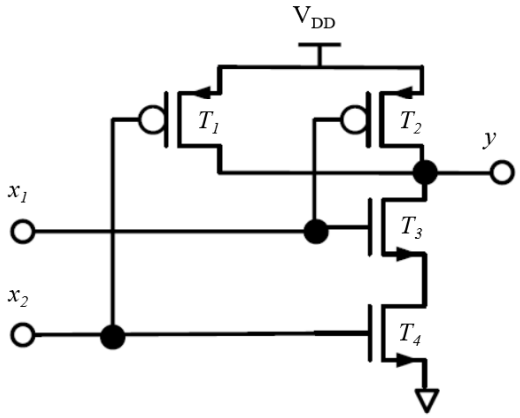
CMOS Logic Gates ("Sea moss?... ?*Sí, mas?* …Yes, CMOS…MOS Definitely!)

1. For the circuit below, consider the two possible states for input x (high = V_{dd} or low = 0V). What is the state (on/off) of each transistor?
2. Complete the table to find the output state *y* for each of two possible input states *x*.
3. Propose a name for this logic gate based on the function encoded in the table above.
4. You're encouraged to watch this video demonstrating this CMOS circuit action using mechanical switches.



x	*pmos state*	*nmos state*	*y*

5. Consider the following CMOS logic gate circuit. Determine the logic it implements by completing the table below. T1 – T4 indicates the state (on/off) of the corresponding transistor. What type of logic does this CMOS circuits implement?



X1	X2	T1	T2	T3	T4	y

6. The XOR gate is a somewhat tricky one to build. Build an XOR gate using any combination and configuration of the first 5 logic gates shown below in Figure 1. Draw the schematic and complete the truth table to illustrate how it works.
7. Then build a CMOS based schematic implementing XOR logic perhaps inspired by your result from part 5.

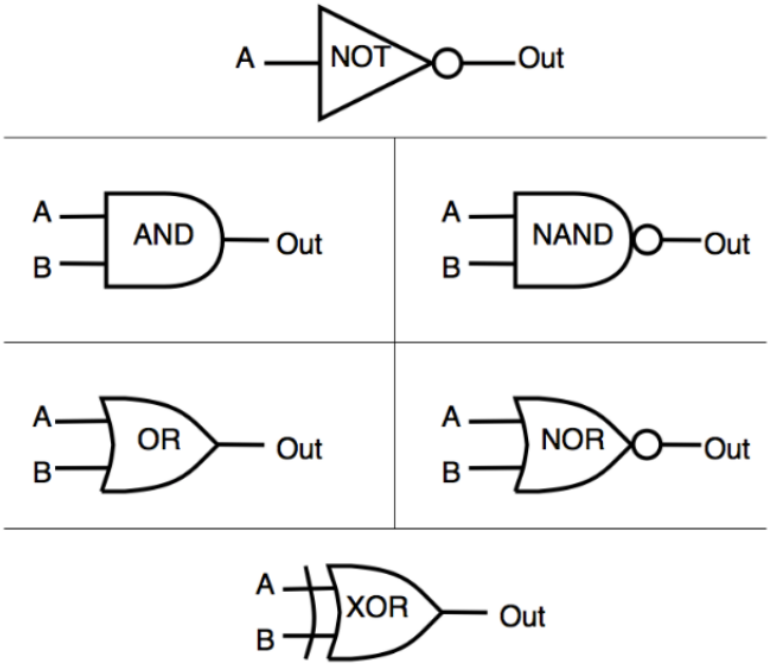


Figure 1. Logic Gate Symbols. The happy family of the 6 standard logic gates. Note the flat vs. curved back differentiating AND and OR. Also note the 'bubbles' indicate inverting logic—e.g. AND vs. NAND.