

SN5400, SN54LS00, SN54S00 SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

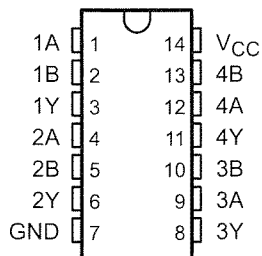
SDLS025B - DECEMBER 1983 - REVISED OCTOBER 2003

- Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package

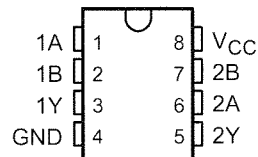
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400, SN74S00 . . . D, N, OR NS PACKAGE
SN74LS00 . . . D, DB, N, OR NS PACKAGE

(TOP VIEW)



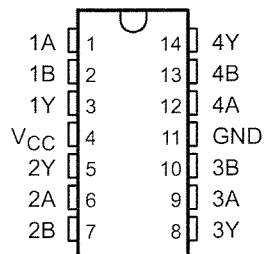
SN74LS00, SN74S00 . . . PS PACKAGE

(TOP VIEW)



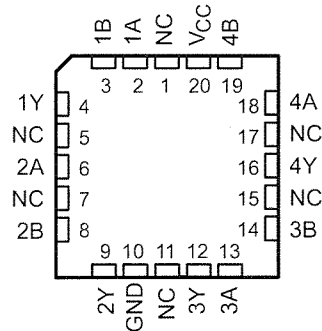
SN5400 . . . W PACKAGE

(TOP VIEW)



SN54LS00, SN54S00 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.



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**TEXAS
INSTRUMENTS**

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**SN5402, SN54LS02, SN54S02,
SN7402, SN74LS02, SN74S02**
QUADRUPL 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

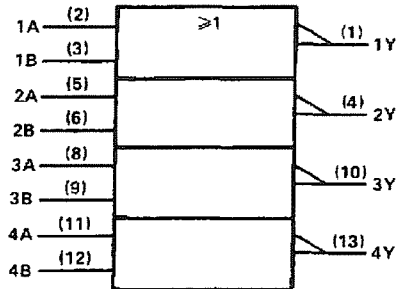
These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

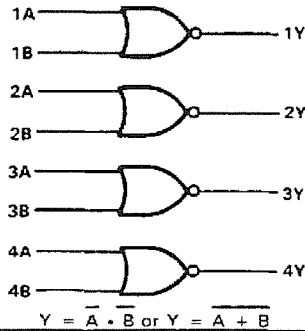
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

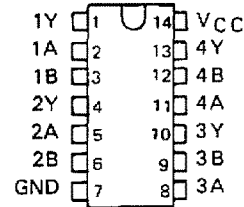
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



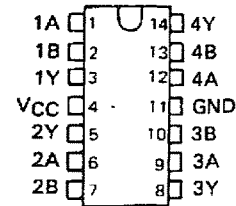
SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE

(TOP VIEW)



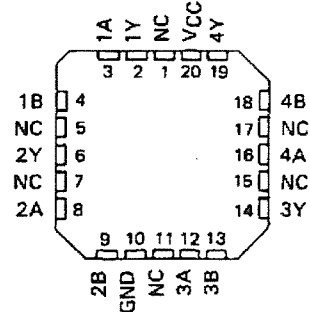
SN5402 . . . W PACKAGE

(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

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SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

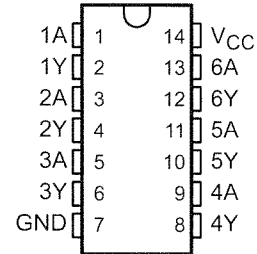
SDLS029C - DECEMBER 1983 - REVISED JANUARY 2004

- Dependable Texas Instruments Quality and Reliability

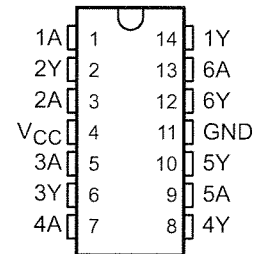
description/ordering information

These devices contain six independent inverters.

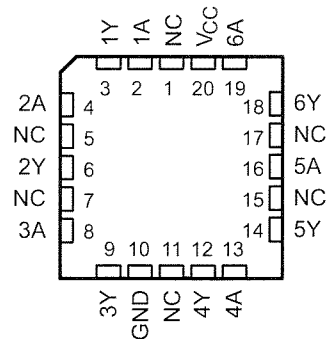
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection



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SN5408, SN54LS08, SN54S08 SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

SDLS033 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

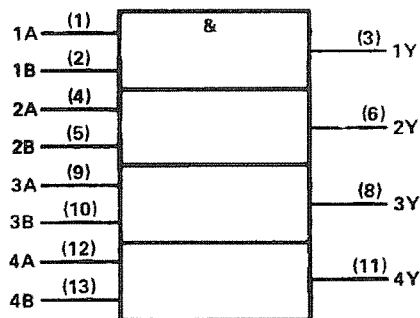
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

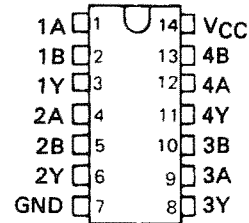


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

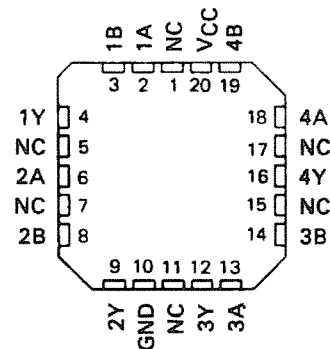
SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE

(TOP VIEW)



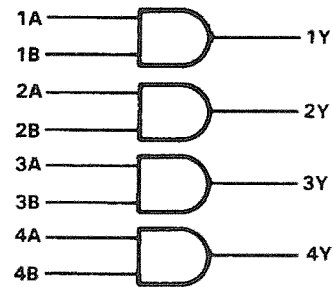
SN54LS08, SN54S08 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic diagram (positive logic)



$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

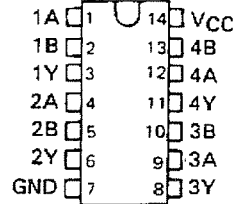
SDLS100

**SN5432, SN54LS32, SN54S32,
SN7432, SN74LS32, SN74S32
QUADRUPLE 2-INPUT POSITIVE-OR GATES**

DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN5432, SN54LS32, SN54S32 . . . J OR W PACKAGE
SN7432 . . . N PACKAGE
SN74LS32, SN74S32 . . . D OR N PACKAGE
(TOP VIEW)



description

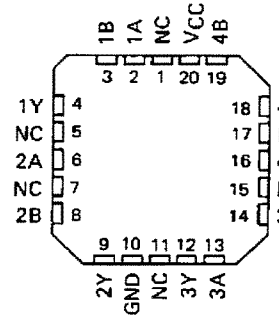
These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

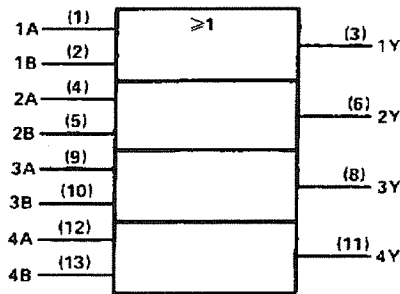
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

SN54LS32, SN54S32 . . . FK PACKAGE
(TOP VIEW)



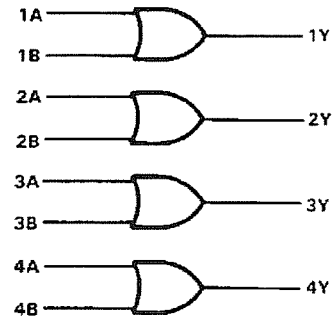
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, or W packages.

NC - No internal connection

logic diagram




positive logic

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

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FAIRCHILD
SEMICONDUCTOR INC.

September 1986
Revised February 2000

DM7486

Quad 2-Input Exclusive-OR Gate

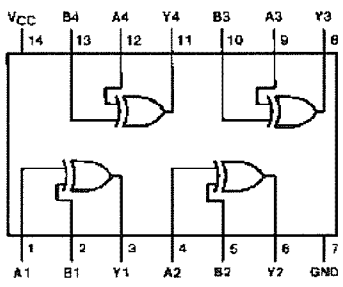
General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM7486N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

DM7486 Quad 2-Input Exclusive-OR Gate